



Europäisches Patentamt

European Patent Office

Office européen des brevets

(11) Publication number:

0 175 152
A3

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 85110330.8

(51) Int. Cl. 4: G 05 F 3/20

(22) Date of filing: 19.08.85

(30) Priority: 21.08.84 US 642837

(71) Applicant: LATTICE SEMICONDUCTOR CORPORATION
10300 SW Greenburg Road
Portland Oregon 97223(US)

(43) Date of publication of application:
26.03.86 Bulletin 86/13

(72) Inventor: Moench, Jerry D.
11305 Spicewood Parkway
Austin Texas 78750(US)

(88) Date of deferred publication of search report: 20.11.86

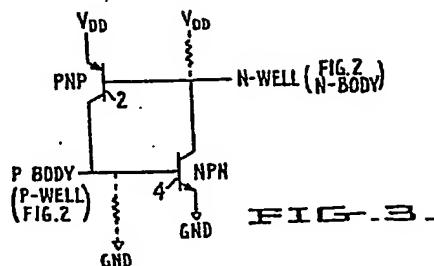
(72) Inventor: Tesch, Rodney C.
9830 S.W. Buckskin Terrace
Beaverton Oregon 97005(US)

(84) Designated Contracting States:
DE FR GB IT

(74) Representative: Bernhardt, Klaus
Radeckestrasse 43
D-8000 München 60(DE)

(64) A method and an apparatus to prevent latchup in a CMOS device.

(57) An apparatus and a method is disclosed to prevent latchup in a CMOS device and, in particular, during the power-up phase of the CMOS device. A switching transistor is interposed between the power V_{DD} and the P-channel transistors. A control circuit controls the switching transistor, such that the switching transistor is turned off when power is initially applied to the CMOS device. The substrate of either the N channel MOS transistor or the P channel MOS transistor, preferably both, is biased with the latter being biased above V_{DD} and the former being biased to a negative potential. Once the substrate of the N channel MOS transistor and the P channel MOS transistor are biased, the switching transistor is then turned on permitting power to be applied to the P channel transistors.



EP 0 175 152 A3



European Patent
Office

EUROPEAN SEARCH REPORT

0175152

Application number

EP 85 11 0330

DOCUMENTS CONSIDERED TO BE RELEVANT		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Category	Citation of document with indication, where appropriate, of relevant passages		
X	US-A-4 039 869 (RCA) * Column 2, line 7 - column 3, line 18; column 4, lines 40-62; figure 1 *	1-3, 7, 9, 10	G 05 F 3/20
A	US-A-4 260 909 (BELL) * Abstract; figure 1 *	1, 4, 8	
A	US-A-4 109 161 (NEC) * Abstract; column 1, line 58 - column 2, line 4; figure 1 *	1, 7, 9, 12	
A	EP-A-0 036 494 (SIEMENS) * Abstract; figure 1 *	1	
A	IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, 13th February 1980, pages 58, 59, New York, US; A.C. GRAHAM et al.: "Battery backup circuits for memories" * Whole document *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4). G 05 F 3/00 H 02 M 3/00 H 01 L 27/08
A	PATENTS ABSTRACTS OF JAPAN, vol. 7, no. 140 (E-182)[1285], 18th June 1983; & JP - A - 58 52 869 (NIPPON DENKI K.K.) 29-03-1983 * Whole abstract *	5, 6	
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	25-08-1986	ZAEHEL B.C.	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone	Y : particularly relevant if combined with another document of the same category		
A : technological background	O : non-written disclosure		
P : intermediate document			